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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,365	01/22/2004	Taro Fujii	Q79526	3414

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,365	FUJII ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-15 are pending.

Papers Filed

Examiner acknowledges receipt of remarks, claim amendments, and interview summary filed on 26 September 2008.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 September 2008 has been entered.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

In general, specification language should be revised to improve readability, comprehensibility and grammar. Doing so may increase enforceability of any future patent that results from this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl et al. (U.S. Patent No. 5,710,938) in view of Toll (U.S. Patent No. 6,308,279).

2. As per claim 1, Dahl teaches an array-type processor comprising

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, said multiplicity of processor elements arranged in rows and columns, (Fig. 1) and a state control unit (Fig. 1 controller 20) which changes a configuration of the multiplicity of processor elements and causes successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas; (Figs. 2a, 2b and 2c and col. 1 lines 42-57)

one said state control unit is connected to the plurality of element areas; *Controller 20 in Fig. 1 is shown as being connected to all of the processing elements.*

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; *The examiner asserts that instructions passed to the processing elements cause them to change operations.*

and said state control unit temporarily halts operations of said element areas that correspond to a prescribed number of said operating states that are set to one said context during said operating cycles in which said operating states do not occur. *When a processing element (or group of elements) does not have a task to perform (operating state), it will inherently halt processing. Inherently, the processor must be told to start processing by passing it some sort of instruction (context).*

Dahl fails to disclose that the control unit individually halts the plurality of element areas.

Toll discloses the use of a "stop grant mode" which halts individual processors or individual threats of a multiprocessor system (col 2 lines 19-34 and 52-55).

Dahl would have been motivated to utilize the technique of Toll in order to more effectively conserve power when the resources of a particular element area are not needed.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Dahl and incorporate the stop grant mode of Toll.

3. As per claim 2, Dahl/Toll teaches an array-type processor comprising

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set said multiplicity of processor elements arranged in rows and columns, (Fig. 1) and state control units (Fig. 1 controller 20) which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas; (Figs. 2a, 2b and 2c and col. 1 lines 42-57)

each of the plurality of element areas is connected to a respective state control unit of an equal number of the element areas; *The examiner asserts that each element area is connected to controller 20, as shown in fig. 1. Inherently, the controller will be connected to any number of element areas that the processing elements are split into.*

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; *The examiner asserts that instructions passed to the processing elements cause them to change operations.*

and said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur.

Said plurality of state control units individually and temporarily halt said plurality of element areas (Toll col 2 lines 19-34 and 52-55).

4. As per claim 3, Dahl/Toll teaches an array-type processor comprising

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, said multiplicity of processor elements arranged in rows and columns, and state control units (Fig. 1 controller 20) which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a number (a x b) of element areas; (Fig. 2a, 2b, 2c and col. 1 lines 42-57)

each of a number (a) of said state control units is connected to a respective group of (b) element areas of these (a x b) element areas; *The examiner asserts that Dahl/Toll discloses the instance where there is one element area and one controller, as shown in fig. 1.*

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; *The examiner asserts that instructions passed to the processing elements cause them to change operations.*

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas

corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur.

Said plurality of state control units individually and temporarily halt said plurality of element areas (Toll col 2 lines 19-34 and 52-55).

5. As per claims 4-6, Dahl/Toll teaches an array-type processor according to claims 1-3, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted. *The examiner asserts that Dahl/Toll's processor will inherently restart processing in any elements that have previously been halted when they are needed for a subsequent operation. If this were not the case, the processor would lose functionality as processing elements halted.*

6. As per claims 7-12, Dahl/Toll teaches an array-type processor according to claims 1-6, wherein:

a shared resource is provided that is shared by said plurality of element areas; *Memory element 22 (fig. 1) is shared by all processing elements. (Col. 6 line 43)*

and said state control units switch paths to said shared resource from said plurality of element areas. *Paths must inherently be switched by message routing circuits (Fig. 1 element 10) in order for the processing elements to receive their proper messages.*

7. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl/Toll in view of .Chauvel (U.S. Patent No. 6,901,521).

8. Regarding claims 13-15, Dahl/Troll discloses the array-type processor according to claims 1-3, but fails to indicate that the processing elements are on a single substrate.

Chauvel discloses a more modern trend of putting multiple processors on a single integrated circuit (col 1 lines 49-58).

Dahl/Toll would have been motivated to follow this trend to address more complicated applications and take advantage of the efficient nature of integrated circuits.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Dahl/Toll and allow the multiple processors to be integrated on a single circuit, as in Chauvel.

Response to Arguments

Applicant's arguments filed 26 September 2008 have been fully considered but they are not persuasive.

Applicant argues that Dahl contains an array of individual processors while the claimed invention requires an array processor with individual processing elements. The questions become: can a general purpose processor within the context of an array be

reasonable interpreted as a processing element? And can the collection of these processors be reasonably interpreted as an array processor? To answer these questions, Examiner looks toward the characterization of these elements in previously published patents. Upon further review, the answers to these questions appear to be yes (Gay-Bellile, U.S. Patent No. 6,862,325, col 6 lines 57-61) and yes (Dieffenderfer, U.S. Patent No, 5,822,608, col 6 lines 40-46). Indeed, the definition of a processor according to the American Heritage Science Dictionary is "[a] part of a computer, such as the central processing unit, that performs calculations or other manipulations of data." A processing element, as described in Applicant's specification, certainly fits the definition of a processor. Whether it is called a "processing element" or a "processor" is no more than an issue of semantics.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian Johnson/ Patent Examiner, Art Unit 2183

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183